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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/533,715	05/03/2005	Hans-Helmut Bechtel	DE 020248	7791
24737 7590 03/28/2008 PHILIPS INTELLECTUAL PROPERTY & STANDARDS P.O. BOX 3001 BRIARCLIFF MANOR, NY 10510				
EXAMINER SANTIAGO, MARICELI				
ART UNIT 2879		PAPER NUMBER		
MAIL DATE 03/28/2008		DELIVERY MODE PAPER		

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/533,715

Applicant(s)

BECHTEL ET AL.

Examiner

Mariceli Santiago

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-10 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-7, 9 and 10 is/are rejected.
- 7) ☒ Claim(s) 8 is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 03 May 2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. ____.
 - ☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/ISD)
- 4) ☐ Interview Summary (PTO-413)
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: ____
- Paper No(s)/Mail Date 5/05, 3/06

DETAILED ACTION

Response to Amendment

Receipt of the Amendment, filed on May 3, 2008, is acknowledged.

Claims 1-10 are pending in the instant application.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4 are rejected under 35 U.S.C. 102(b) as being anticipated by Nakabachi et al. (JP 05-029082 A).

Regarding claim 1, Nakabachi discloses a display device comprising a first electrode (2) and a second electrode (7), and an optical layer (4) arranged between the electrodes, which optical layer emits light under the influence of an electric field applied between the electrodes, and comprising a varistor layer (5) arranged between an electrode (7) and the optical layer (4).

Regarding claim 2, Nakabachi discloses a display device characterized in that the varistor layer is structured and situated in the areas where the first electrode (2) and the second electrode (7) overlap one another.

Regarding claim 3, Nakabachi discloses a display device characterized in that the varistor layer (5) is arranged parallel to the optical layer (4), and the surface over which the varistor layer extends corresponds to the surface over which the optical layer extends (Fig. 1).

Regarding claim 4, Nakabachi discloses a display device characterized in that a dielectric layer is situated between the optical layer and the varistor layer (not shown in drawing,

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¶[0009] states positioning the varistor layer between the ITO film and the 1st insulator layer, between the 1st insulator layer and a fluorescence layer, or between the 2nd insulator layer and an electrode).

Claims 1-6 are rejected under 35 U.S.C. 102(b) as being anticipated by Kano et al. (US 6,198,225).

Regarding claim 1, Kano discloses a display device (Fig. 21) comprising a first electrode (374) and a second electrode (384), and an optical layer (382) arranged between the electrodes, which optical layer emits light under the influence of an electric field applied between the electrodes, and comprising a varistor layer (375) arranged between an electrode (374) and the optical layer (382).

Regarding claim 2, Kano discloses a display device characterized in that the varistor layer is structured and situated in the areas where the first electrode (374) and the second electrode (384) overlap one another.

Regarding claim 3, Kano discloses a display device characterized in that the varistor layer (375) is arranged parallel to the optical layer (382), and the surface over which the varistor layer extends corresponds to the surface over which the optical layer extends (Fig. 21).

Regarding claim 4, Kano discloses a display device characterized in that a dielectric layer (380) is situated between the optical layer (382) and the varistor layer (375).

Regarding claim 5, Kano discloses a display device characterized in that the dielectric layer comprises a dielectric material having a dielectric constant $\epsilon > 20$ (It is noticed that although Kano does not explicitly state the dielectric constant of the dielectric layer 380, the materials used by Kano are known to have a dielectric constant greater than 20).

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Regarding claim 6, Kano discloses a display device characterized in that the varistor layer substantially comprises ZnO doped with at least one material selected from the group consisting of Bi₂O₃, CO₂O₃, MnO₂, Sb₂O₃, Al₂O₃ and B₂O₃ (Column 27, lines 29-46).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakabachi et al. (JP 05-029082 A) in view of Masuyama et al. (US 4,545,929).

Regarding claim 7, Nakabachi fails to exemplify the materials use for the varistor layer. However, Masuyama discloses ceramic materials having voltage-dependent nonlinear resistance, i.e. varistors, and further acknowledges the varistor layer substantially comprises SrTiO₃ doped with at least one material selected from the group consisting of La₂O₃, Nb₂O₅ and WO₃ (abstract). It is considered within the capabilities of one skilled in the art the selection of a material based on its known suitability for an intended application as an obvious matter of design engineering. Thus, it would have been obvious to one having ordinary skills in the art at the time the invention was made to use the ceramic material having voltage-dependent nonlinear resistance disclosed by Masuyama as the varistor layer material of Nakabachi, since the selection of known materials for a known purpose is within the skill of the art.

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakabachi et al. (JP 05-029082 A) in view of Greuter et al. (US 5,858,533).

Regarding claim 9, Nakabachi fails to exemplify the materials use for the varistor layer. However, Greuter discloses a composite material for a varistor layer comprising a polymeric matrix in which either ZnO particles or SrTiO₃ are doped (Column 2, lines 50-53; Column 3, lines 1-12). It is considered within the capabilities of one skilled in the art the selection of a material based on its known suitability for an intended application as an obvious matter of design engineering. Thus, it would have been obvious to one having ordinary skills in the art at the time the invention was made to use the polymeric ZnO/ SrTiO₃ doped material having voltage-dependent nonlinear resistance disclosed by Greuter as the varistor layer material of Nakabachi, since the selection of known materials for a known purpose is within the skill of the art.

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakabachi et al. (JP 05-029082 A) in view of Chakrabarty et al. (US 4,186,367).

Regarding claim 10, Nakabachi discloses a method of manufacturing a display device comprising a first electrode (2) and a second electrode (7), and an optical layer (4) arranged between the electrodes, which optical layer emits light under the influence of an electric field applied between the electrodes, and comprising a varistor layer (5) arranged between an electrode (7) and the optical layer (4). Nakabachi fails to exemplify the step of the varistor layer being applied by means of blade coating or screen printing. However, Chakrabarty discloses a method of manufacturing and coating a varistor layer by using a screen printing technique, the varistor layer is manufactured from a glass-free particulate mixture having good adhesion to the deposition surface, and improved electrical characteristics. Thus, it would have been obvious at

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the time the invention was made to a person having ordinary skills in the art to incorporate the manufacture and deposition technique of the varistor element disclosed by Chakrabarty in the method Nakabachi in order to provide a thick varistor layer having good adhesion to the deposition surface, and improved electrical characteristics.

Allowable Subject Matter

Claim 8 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 8, the references of the Prior Art of record fails to teach or suggest the combination of the limitations as set forth in claim 8, and specifically comprising the limitation of the varistor layer substantially comprises YTiO_3 doped with at least one material selected from the group consisting of La_2O_3 , Nb_2O_5 and WO_3 .

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mariceli Santiago whose telephone number is (571) 272-2464. The examiner can normally be reached on Monday-Friday from 9:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nimesh Patel, can be reached on (571) 272-2457. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications

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may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Mariceli Santiago/

Primary Examiner, Art Unit 2879